mm-Wave and sub-THz Chip-to-Package Transitions for Communications Systems

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Abstract—This work presents mm-Wave and sub-THz chipto-package transitions for communications systems. To date, reported transitions either have high loss, typically $3-4\,\mathrm{dB}$, or require high cost packages to support very fine bump pitches and low loss materials. We analyze the impact of transitions on a high frequency, wide bandwidth communication system and present the design of a chip-to-package transition in two different commercial packaging technologies. The proposed transitions achieve $\leq 1\,\mathrm{dB}$ loss in both technologies, validating the design methodology.

Index Terms—CMOS integrated circuits, packaging, interposer, interconnect, mm-Wave, sub-THz.

I. INTRODUCTION

THE transition of signal from an integrated circuit (IC) to printed circuit board (PCB) becomes increasingly difficult and costly as the signal frequency increases. Wire bond inductance becomes a limiting factor in the achievable bandwidth [1] and at high frequency, transitions can excite radiation and other parasitic waveguide modes, which leads to notches in the transmission characteristic. Flip-chip technology [2] and an interposer between the IC and PCB [3] support finer feature sizes, however this comes at higher costs that impact high-volume manufacturing. These factors lead to transitions having high loss, typically $3 - 4 \,\mathrm{dB}$, or requiring costly packaging technologies [4], [5], [6]. With the trend towards large phased arrays or massive multiple-input multiple-output (MIMO) antenna arrays to compensate for high frequency path losses, the integration of transceivers with antenna elements becomes a challenge. While on-chip antennas eliminate the need to transition from the IC to the PCB, due to the excitation of substrate waves and ohmic losses, radiation efficiency and gain remain low [7], [8]. With these challenges, the design of low loss and broadband chip-to-package transitions in low cost packaging technologies, as shown in Fig. 1, is crucial for future communications and sensing systems.

This article is organized as follows. This section (Section I) motivates technology choices and examines system performance in lieu of chip-to-package transitions. Section II analyzes the limitations of typical transition structures and provides design methodology for alternative structures. Finally experimental measurements are described in Section III.



1

Fig. 1. A flip-chip CMOS chip-to-package transition on a low-cost organic substrate interposer for mm-Wave and sub-THz communication systems.

A. Technology Choice

The mm-Wave and sub-THz bands have gained interest for use in future communications and radar/sensing systems for the large available bandwidths that can be utilized to increase data rates or increase resolution in imaging/radar. Despite the higher $f_T/f_{\rm max}$ of III-V material-based technologies, advances in CMOS technology have enabled their application to mm-Wave and sub-THz frequencies. The high yield and low cost of CMOS, along with high integration density, make it the attractive technology for future integrated communication systems. Regardless of technology, arrays of transceivers are required to compensate for additional path losses at these frequencies. This poses an integration challenge for massive arrays of transceivers. While this could be mitigated with the use of on-chip antennas, due to substrate surface waves and ohmic losses on-chip antennas have low gain and low radiation efficiency [9], [10], [11]. Furthermore, since most anntena arrays have an element spacing of $\lambda/2$, the transceiver area becomes a limiting factor. Antenna-integrated packages offer higher gain and radiation efficiency, while supporting large integration needs of massive arrays [7].

The technology of choice for antenna-integrated packages greatly affects performance and cost. As signal wavelengths decrease, the required pitch for chip bumps and package balls to maintain signal integrity decreases, requiring tighter manufacturing tolerances. While low-temperature co-fired ceramic

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(LTCC), laminate, or even silicon-based package technologies can offer lower loss or higher integration density, this comes at added cost and thermal/mechanical considerations due to thermal expansion mismatch between materials. Meanwhile organic substrates provide multilayered packages that utilize similar manufacturing techniques as traditional PCB processes, but still provide sufficient pitch for use with ICs and lower loss than connecting directly to the PCB. This makes them an attractive alternative to other packaging options [3].

An additional benefit of supporting direct chip-to-package transitions at these high frequencies is the possibility of heterogeneous integration of blocks in the core transceiver. While CMOS has clear advantages over other technologies in terms of cost (in volume) and yield, III-V technologies such as indium phosphide (InP) or galium nitride (GaN) still offer superior output power as compared to CMOS. By facilitating the transition from chip-to-package, the possibility to integrate multiple technologies together in a single transceiver becomes feasible, providing the best cost and performance for a single system.

B. Link Budget

As communication systems seek to increase bandwidth, link capacity becomes more sensitive to changes in signal-tonoise ratio (SNR). In particular losses before the low-noise amplifier (LNA) in a receiver and after the power amplifier (PA) in a transmitter, both of which directly degrade SNR, will cause greater variation in throughput than in lower bandwidth systems. These losses typically are dominated by link path loss and interface losses between the transceiver IC and the antenna. The former is out of control of the designer when targeting a particular system application, while the latter is in the designer's control.

Suppose a base station has an N_{ant} -antenna phased array with N_{pol} polarizations operating at a bandwidth B with N_{beams} beams, where one beam is equivalent to one user. The total SNR of the transceiver can be estimated as

$$SNR = \frac{P_{tx}G_t N_{ant}^2}{4\pi d^2 I L_{PCB}} \frac{c^2 G_r N_{ant}^2}{4\pi f_0^2 I L_{PCB}} \frac{1}{k_B T B F N_{ant}}$$
(1)

where the first term is the transmitted power density, the second term is the effective receiver area, and the third term is the received noise power. In Eq. (1) P_{tx} is the transmitted power after back-off; G_t is the transmit antenna gain; d is the link distance; IL_{PCB} is the insertion loss due to chip-to-package interfaces; c is the speed of light in vacuum; G_r is the receive antenna gain; f_0 is the center frequency of operation; k_B is Boltzmann's constant; T is the ambient temperature; B is the channel bandwidth; and F is the linear receiver noise factor. A line-of-sight (LoS) link is assumed in Eq. (1). Note that IL_{PCB} is squared in the equation since it simultaneously degrades receiver noise figure and transmitter output power.

With Shannon's capacity theorem, $C = B \log_2 (1 + SNR)$ [12], the capacity per beam per polarization can be estimated.



Fig. 2. The impact of chip-to-package transition losses on link capacity for a proposed wideband systems. Here $f_0 = 140 \text{ GHz}$, B = 20 GHz, $N_{ant} = 16$, $N_{beams} = 8$, $N_{pol} = 2$, $P_{tx} = 4 \text{ dBm}$ after back-off, $G_r = G_t = 5 \text{ dB}$, d = 5 m, and F = 10 dB.

For SNR $\gg 1$, the aggregate capacity is

$$C_{tot} \approx N_{beams} N_{pol} B \log_2\left(\frac{SNR}{N_{beams}}\right)$$
 (2a)

$$\propto N_{beams} N_{pol} B \log_2 \left(1/I L_{PCB}^2 \right).$$
 (2b)

The sensitivity to changes in transition losses can then be calculated to be

$$S_{PCB} \approx -\frac{2\log_2(10)}{10} N_{beams} N_{pol} B \text{ bits/s/dB.}$$
(3)

In a potential future base station, we may have $N_{beams} = 8$, $N_{pol} = 2$, and B = 20 GHz. At 140 GHz this system is under 15% fractional bandwidth, while achieving tera-bit per second capacity. However the resulting sensitivity to packaging loss is approximately 212 Gbits/s/dB. Fig. 2 shows link capacity versus transition loss without the large SNR approximation and highlights the importance of minimizing losses between active devices and the antenna in high bandwidth systems.

II. CHIP-TO-PACKAGE TRANSITIONS

The standard chip-to-package interface is a coplanar groundsignal-ground (GSG) transition. However these transitions become very lossy above 100 GHz. To address the challenges in chip-to-package interface design we analyze the loss mechanisms in the traditional GSG transition, discuss possible alternatives, and present modified designs that achieve broadband and low loss performance in a compact footprint.

A. Limitations of GSG-type Transitions

The GSG transition structure is shown in Fig. 3a. In this structure, a grounded coplanar waveguide (GCPW) on chip transitions to a microstrip line on the PCB or interposer through three flip-chip bumps. Due to the fanout required for bump pitch limitations, the return current travels a longer path than the signal current in this transition, which can be modelled with transmission lines. The cross section and transmission line model of the structure is shown in Fig. 3b and Fig. 3c, respectively. In this model, the bumps that carry current in the vertical direction are intentional transmission



Fig. 3. Conventional microstrip GSG transition (a) structure, (b) cross section, (c) schematic model and (d) simulated Poynting vector at 400 GHz.

lines, shown in red, while the horizontal paths that the return currents must follow on the PCB and chip are parasitic transmission lines, shown in green.

Using this model, the input current into the intended transmission line must equal the input current into the parasitic line. Therefore the currents at either ends of the parasitic transmission line must be the same,

$$I_{in} = \frac{v_{2f} - v_{2r}}{Z_2} = \frac{v_{2f}e^{-j\theta_2} - v_{2r}e^{j\theta_2}}{Z_2} = I_{out} \qquad (4)$$

where v_{xf} and v_{xr} are the voltage of the propagating waves in the forward and reverse directions respectively, Z_x is the characteristic impedance, τ_x is the time delay, and θ_x is the electrical length of each transmission line. To satisfy this equation,

$$e^{j\theta_2} = -\frac{v_{2f}}{v_{2r}}.$$
(5)

From this, the standing wave ratio on the second transmission line does not depend on the load impedance. Moreover, at the frequency where $\theta_2 = \pi$,

$$I_{in} = \frac{v_{2f} - v_{2r}}{Z_2}$$
(6)

$$=\frac{v_{2f}+v_{2f}e^{-j\theta_2}}{Z_2}=0$$
(7)

which suggest that at the frequency

$$f_{\text{notch}} = \frac{1}{2\tau_2} \tag{8}$$

or an odd integer multiple of that, a notch in the transmission characteristic is expected. In other words, the timing mismatch between current and reverse current results in deep notches in the transition. The other transmission line may also exhibit similar notch behavior; however, for most practical transitions $\tau_1 < \tau_2$. This deep notch is easily seen when the length of the horizontal line is much greater than that of the vertical line, which is usually the case when small bumps are used on low manufacturing resolution PCBs.

The derivation above shows a parallel resonance in the circuit due to this propagation delay mismatch. However, since the circuit in Fig. 3c has no loss, it is reasonable to assume this



Fig. 4. GSG simulation showing (a) notches in G_{max} for different pitches and (b) the loop antenna radiation model for the notch frequency.

resonance can be tuned out with ideal reactive components. In practice, however, this strong resonance couples energy to lossy modes, which cannot be recovered by simple reactive tuning. Physically there are two dominant modes. First, since the parasitic transmission line is a 2-D parallel-plate transmission line, the signal can escape by coupling to the parallel-plate propagation mode at the metal-dielectric-metal stack in the transition region, as shown by Poynting vector simulations with Ansys HFSS in Fig. 3d. Second, a parasitic loop antenna is excited at the transition, as shown in Fig. 3b. This loop antenna is in resonance when the circumferential length of the loop is equal to the wavelength, assuming a short circuit on the chip. In terms of delays in the transmission line model

$$f_{rad} = \frac{1}{2(\tau_1 + \tau_2)}.$$
 (9)

The incoming signal near the radiation frequency is dissipated by coupling with parasitic surface wave modes and parallel plate modes, which can be seen by considering G_{max} , the two-port maximum available power gain, in Fig. 4a. It can be observed that as the bump pitch increases, the first notch moves closer to the origin. Here, a bump pitch of 150 µm is considered, which is the minimum bump pitch offered by the technology used. In the simulation structure, the total distance between two footprints (H in Fig. 3b) is 125 µm. With a dielectric constant of 3.1 for the underfill material, Eq. (9) estimates the first notch to be

$$f_{\text{notch}} \approx \frac{1}{2} \frac{\frac{3 \times 10^8 \text{ m/s}}{\sqrt{3.1}}}{125 \,\mu\text{m} + \text{Pitch}} \tag{10}$$

where Pitch is shown in Fig. 3b. As evident by Fig. 4b, the radiation frequency of the loop antenna model agrees well with the simulated notch frequency.



Fig. 5. Comparison between metal and dielectric materials losses and radiation losses in a back-shielded microstrip to chip transition.

As we move to higher frequencies, and lower wavelengths, these radiation losses become more critical when compared to metal and dielectric material losses. As an example, Fig. 5 demonstrates that even in a back-shielded microstrip-to-chip transition, radiation losses dominate beyond 140 GHz. Therefore as we move to higher frequencies, alternative chip-to-package transition structures need to be considered.

B. Alternative Transition Structures

Since GSG transitions are not suitable for high frequencies, we explore alternative structures, which are presented in Fig. 6. Additional ground bumps are added to the structure in Fig. 6a. This can partially reflect surface waves, however the reflected wave will still reach the chip boundary and be dissipated either by radiation or excitation of surface waves, shown in Fig. 6b. To combat this effect, two sets of ground bumps with positive and negative offsets in a rectangular shape can be used to make the transition shown in Fig. 6c. This is a much better approach in the lower frequency range because it can effectively reject forward and backward surface waves. However, as the distance between two ground bumps or the frequency increases, higher leakage is expected, as shown in Fig. 6d. Moreover, as the length of the PCB microstrip line increases over the chip region, this structure suffers from a higher degree of de-tuning and coupling with the silicon substrate.

The previous two structures indicate that the least leakage is expected when a full bump cage is formed with minimal spacing. To achieve this, the ground bumps are placed in a hexagonal pattern surrounding the signal, shown in Fig. 6e. The simulation results shown in Fig. 7 indicate that this structure achieves the best performance in terms of transition loss and notch frequency. Unfortunately, depending on the capabilities of the PCB manufacturer, this design may be impractical since the microstrip signal must be squeezed out of two ground bumps and their associated pads.

If the previous structure with a full shield is not feasible, a reverse microstrip could be used, as in Fig. 6g. In this structure the ground plane is implemented on the second metal layer, while the signal resides on the third metal layer, and the stack-up is shown in Fig. 13d. This shields the signal



Fig. 6. Possible modified transition structures: (a) half-shielded, (c) rectangular shield, (e) fully shield, (g) reverse microstrip, and (i) stripline. The Poynting vector for each corresponding transition at 400 GHz is shown in (b), (d), (f), (h), and (j).

line from coupling with other chip signals or the substrate. Furthermore the transition can be placed in the middle of the chip without interruption of other signals. While this transition structure minimizes leakage at the chip interface, signal losses occur at the inner via. Furthermore at higher frequencies the reverse microstrip can become a radiating element, as shown in Fig. 6h. Moreover, it requires a large keep-out region above the signal line to reduce the parasitic coupling, making it less attractive.

To solve the problem with the previous structures, the microstrip line can be replaced by a stripline, as shown in Fig. 6i. The advantage of the stripline is that the signal is completely shielded from the external environment, mitigating the impact of variations in the shape of the underfill or the expansion of the silicon. The Poynting vector shown in Fig. 6j shows that the fields are contained by this structure.



Fig. 7. G_{max} of the transition structures presented in Fig. 6 from 0-400 GHz.

The performance of the structures discussed is summarized in Fig. 7. While the microstrip with a full shield performs the best, the stripline design provides a practical signal escape and has the superior performance when compared to other practical options.

C. Limitations of the Stripline Structure

The stripline design of Fig. 6i is the most promising solution for high frequencies. Therefore, it is desirable to explore this structure and investigate its possible limitations. The cross section of the stripline is shown in Fig. 8a. The first propagation mode of this structure in Fig. 8c is the intended TEM mode, which has no cut-off frequency. However, as the frequency increases, the metal cage around the line forms an effective waveguide, commonly called a substrate-integrated waveguide. Note that the discrete nature of microvias allows only TE propagation modes in the waveguide [13], [14]. The effective width of the waveguide can be approximated by [15]

$$W_{eff} \approx W - \frac{D^2}{0.95P} \tag{11}$$

where W is the center-to-center spacing of the microvias on two sides, D is the diameter of the vias, and P is the spacing of the vias on the same side. The first TE mode of this effective waveguide is shown in Fig. 8d, with a cut-off frequency of 300 GHz. While an ideal straight stripline will perform smoothly in a simulation platform, any other structure may exhibit unpredictable performance above cut-off if the exact length of the transmission lines is not known at the design stage. Therefore, it should be ensured that the cut-off frequency of the TE mode is well above the highest frequency range of interest.

Considering Fig. 7, since lossy resonant modes result in notches in G_{max} , an eigenmode solver of Ansys HFSS was used to study these loss mechanisms. The structure was modified to remove the access transmission lines. Among the numerous resonant modes, one of the modes corresponds to the cavity where the signal goes down through microvias



Fig. 8. The (a) actual and (b) simplified cross section of a stripline substrateintegrated waveguide, as well as the (c) first TEM and (d) second TE propagation modes. The TE mode has a cutoff frequency of $300\,{\rm GHz}$

in the shielded cage, which couples to the TE mode of the parasitic stripline waveguide. Depending on the reflection phase of the coupled wave, the resonant frequency of the loaded structure changes slightly. The actual reflection phase is unknown because this parasitic mode is not necessarily terminated with an actual load. Therefore, the waveguide is short-circuited at the end of the stripline, and several different lengths of the stripline are simulated.

The electric fields are shown in Fig. 9a,b. Note that the phase constant of the TE mode approaches 0 near the cut-off frequency of the waveguide. Once the resonant frequency of the cavity is shifted down towards the cut-off frequency of the waveguide, the phase shift of the reflected wave becomes independent of the length, and therefore the notch in G_{max} will not cross the TE cut-off frequency, as shown in Fig. 9c. While other waveguide modes may be excited, they will occur above 300 GHz, and therefore have no effect on the performance of the transition below 200 GHz.



Fig. 9. The results of eigenmode analysis of the stripline structure. The electric field magnitude for a (a) short line and (b) long line are shown. The resulting notch frequency of the stripline transition with varying stripline length is shown in (c). The variation below the TE mode cutoff frequency due to line length is negligible.



Fig. 10. The (a) side view of the stripline transition and the (b) corresponding circuit model.

D. Simulation Results

Given the advantages of the stripline transition over its counterparts, it was chosen for two chip-to-package transitions in two sets of different chip and package technologies. Below 300 GHz, the transition can be modeled with two capacitors and a series transmission line representing the pad capacitance, the effective delay, and the characteristic impedance of the microvias from the stripline opening to the chip, as shown in Fig. 10.

The first design is with a 28 nm Bulk CMOS technology and an organic substrate interposer. To utilize the full silicon area, a matching network is implemented within the ground cage. It consists of two symmetrical transmission lines shown in Fig. 11a, whose characteristic impedance and length are calculated to obtain a matched impedance at 140 GHz. The performance is shown in Fig. 11b, and the transition achieves 1.03 dB loss with a 85 GHz 3 dB bandwidth.

The second design transitions utilizes a 16 nm FinFET CMOS technology to an organic substrate interposer. In order to lower the loss and improve the bandwidth, the matching transmission line is not integrated directly in the ground shielding bumps. The geometry is shown in Fig. 12a, and the performance is shown in Fig. 12b. Matching is implemented



Fig. 11. The (a) geometry of the transition from 28 nm Bulk CMOS technology to an organic substrate interposer, including integrated symmetrical transmission line matching, and the (b) corresponding transition performance designed for 140 GHz.



Fig. 12. The (a) geometry of the transition from 16 nm FinFET CMOS technology to an organic substrate interposer and the (b) corresponding transition performance designed for 200 GHz.

as an approximately 26Ω line with an electrical length of 31° at 200 GHz. The transition has an insertion loss of 0.41 dB with a 3 dB bandwidth from DC to 339 GHz. The notch in G_{max} corresponds with the cutoff frequency of the TE mode of the stripline, as discussed in Section II-C.



Fig. 13. The (a) 28 nm Bulk CMOS die photo, (b) corresponding assembled organic substrate package, as well as (c) the layout of metal three, where the stripline signal traces reside. Reflect denotes either a short or open, following TRL naming conventions. Relevant part of the stackup is shown in (d). BEOL stands for back end of the line.



Fig. 14. The (a) chip-to-package transition measurement setup and (b) the schematic diagram of the setup. The initial calibration plane from on-package TRL is shown, as well as the reference plane after de-embedding the package feed lines.

III. MEASUREMENTS

The validation of the analysis in Section II-A and Section II-B as well as the simulations in Section II-D was carried out through measurements of back-to-back transitions of the 28 nm Bulk CMOS design. A fabricated die photo is shown in Fig. 13a, showing a line, through, and three reflects from top to bottom. The assembled organic substrate package is shown in Fig. 13b. In addition to the fan-out lines from the chip, the package contains custom stripline thru-reflect-line (TRL) calibration standards.

The measurement setup is shown in Fig. 14. Initially TRL



Fig. 15. The measured propagation constant $\gamma = \alpha + j\beta$, where β is in deg/mm and α is in dB/mm.



Fig. 16. The measurement results of the back-to-back transition with a 1.2 mm on-chip transmission line between transitions.

calibration is performed with the calibration on the package. After calibration, the resulting S-parameters are in the reference impedance of the measured striplines, since there is no well-defined load present on the package. Therefore the propagation constant of the lines can easily be extracted from $S_{21} = e^{-\gamma l}$ of the long 18.72 mm and 10.17 mm lines on the package. The average propagation constant of the two lines is shown in Fig. 15.

With the package transmission line properties determined, 9.5 mm of line is deembedded from the on-chip back-to-back transition structure. The deembedded S-parameters are shown in Fig. 16 and correspond well with simulations, which model surface roughness with the Huray parameters of a $0.25 \,\mu\text{m}$ nodule radius and a surface area ratio of 4 [16]. The deviation in reflection coefficient corresponds to $\lambda/2$ every 9 GHz, which for $\epsilon_r = 3.1$ corresponds to the line length deembedded from the package measurements. The total loss of the backto-back structure is 5.7 dB, which includes the 1.21 mm line on-chip.

IV. CONCLUSION

The transition from transceiver, on IC, to antenna, on package or PCB, is critical for future broadband communication systems. To address this, two transitions were demonstrated

	[5]	[4]	[6]	This Work	This Work
Package Technology	LTCC GL771	RO4350	IPD Carrier	ABF GL102	Organic substrate
Chip Technology	22 nm SOI CMOS	55 nm SiGe HBT	90 nm CMOS	28 nm Bulk CMOS	16 nm FinFET CMOS
Interconnect	Copper Pillar	Copper Pillar	Gold Bump	Solder Bump	Copper Pillar
Bump Size (µm)	30	-	65	75	62
Bump Pitch (µm)	175	-	170	150	156
Center Frequency (GHz)	135	130	163	140	200
Insertion Loss (dB)	1.1	3.0	2.8	1.0	0.4
3 dB Bandwidth (GHz)	180*	-	170†	85	339
Matching 10 dB Bandwidth (GHz)	N/A	-	200	43	90

TABLE I

CHIP-TO-PACKAGE TRANSITION COMPARISON TABLE.

 * 2 dB bandwidth; † Estimated from graph; – Not provided

in low cost CMOS and organic substrate technologies that achieve sub-dB loss over a large bandwidth. Table I shows a comparison of these transitions with other recent publications. Despite using large dimensions typical of low cost packaging or PCB solutions, the proposed and demonstrated transitions offer competitive performance.

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REFERENCES

- [1] V. Valenta, T. Spreng, S. Yuan, W. Winkler, V. Ziegler, D. Dancila, A. Rydberg, and H. Schumacher, "Design and experimental evaluation of compensated bondwire interconnects above 100 GHz," *International Journal of Microwave and Wireless Technologies*, vol. 7, no. 3-4, pp. 261–270, Jun. 2015.
- [2] W. Heinrich, "The flip-chip approach for millimeter wave packaging," *IEEE Microwave Magazine*, vol. 6, no. 3, pp. 36–45, Sep. 2005.
- [3] A. O. Watanabe, M. Ali, S. Y. B. Sayeed, R. R. Tummala, and M. R. Pulugurtha, "A Review of 5G Front-End Systems Package Integration," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 1, pp. 118–133, Jan. 2021.
- [4] M. Sawaby, N. Dolatsha, B. Grave, C. Chen, and A. Arbabian, "A Fully Packaged 130-GHz QPSK Transmitter With an Integrated PRBS Generator," *IEEE Solid-State Circuits Letters*, vol. 1, no. 7, pp. 166–169, Jul. 2018.
- [5] A. A. Farid, A. S. H. Ahmed, A. Simsek, and M. J. W. Rodwell, "A Packaged 135GHz 22nm FD-SOI Transmitter on an LTCC Carrier," in 2021 IEEE MTT-S International Microwave Symposium (IMS), Jun. 2021, pp. 713–716.
- [6] C.-H. Li, W.-T. Hsieh, and T.-Y. Chiu, "A Flip-Chip-Assembled W-Band Receiver in 90-nm CMOS and IPD Technologies," *IEEE Transactions* on Microwave Theory and Techniques, vol. 67, no. 4, pp. 1628–1639, Apr. 2019.
- [7] T. Maiwald, T. Li, G.-R. Hotopan, K. Kolb, K. Disch, J. Potschka, A. Haag, M. Dietz, B. Debaillie, T. Zwick, K. Aufinger, D. Ferling, R. Weigel, and A. Visweswaran, "A Review of Integrated Systems and Components for 6G Wireless Communication in the \$D\$ -Band," *Proceedings of the IEEE*, pp. 1–37, 2023.
- [8] H.-J. Song and N. Lee, "Terahertz Communications: Challenges in the Next Decade," *IEEE Transactions on Terahertz Science and Technology*, vol. 12, no. 2, pp. 105–117, Mar. 2022.
- [9] S. Pan and F. Capolino, "Design of a CMOS On-Chip Slot Antenna With Extremely Flat Cavity at 140 GHz," *Antennas Wirel. Propag. Lett.*, vol. 10, pp. 827–830, 2011.
- [10] S. Hu, Y.-Z. Xiong, B. Zhang, L. Wang, T.-G. Lim, M. Je, and M. Madihian, "A SiGe BiCMOS Transmitter/Receiver Chipset With On-Chip SIW Antennas for Terahertz Applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2654–2664, Nov. 2012.

- [11] S. Pan, L. Gilreath, P. Heydari, and F. Capolino, "Investigation of a Wideband BiCMOS Fully On-Chip \$W\$-Band Bowtie Slot Antenna," *Antennas Wirel. Propag. Lett.*, vol. 12, pp. 706–709, 2013.
- [12] C. E. Shannon, "A mathematical theory of communication," *The Bell System Technical Journal*, vol. 27, no. 3, pp. 379–423, Jul. 1948.
- [13] D. Deslandes and K. Wu, "Integrated microstrip and rectangular waveguide in planar form," *IEEE Microwave and Wireless Components Letters*, vol. 11, no. 2, pp. 68–70, Feb. 2001.
- [14] K. Wu, D. Deslandes, and Y. Cassivi, "The substrate integrated circuits a new concept for high-frequency electronics and optoelectronics," in 6th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Service, 2003. TELSIKS 2003., vol. 1, Oct. 2003, pp. P–III.
- [15] Y. Cassivi, L. Perregrini, P. Arcioni, M. Bressan, K. Wu, and G. Conciauro, "Dispersion characteristics of substrate integrated rectangular waveguide," *IEEE Microwave and Wireless Components Letters*, vol. 12, no. 9, pp. 333–335, Sep. 2002.
- [16] S. Hall, S. G. Pytel, P. G. Huray, D. Hua, A. Moonshiram, G. A. Brist, and E. Sijercic, "Multigigahertz Causal Transmission Line Modeling Methodology Using a 3-D Hemispherical Surface Roughness Approach," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 12, pp. 2614–2624, Dec. 2007.